FIG.1

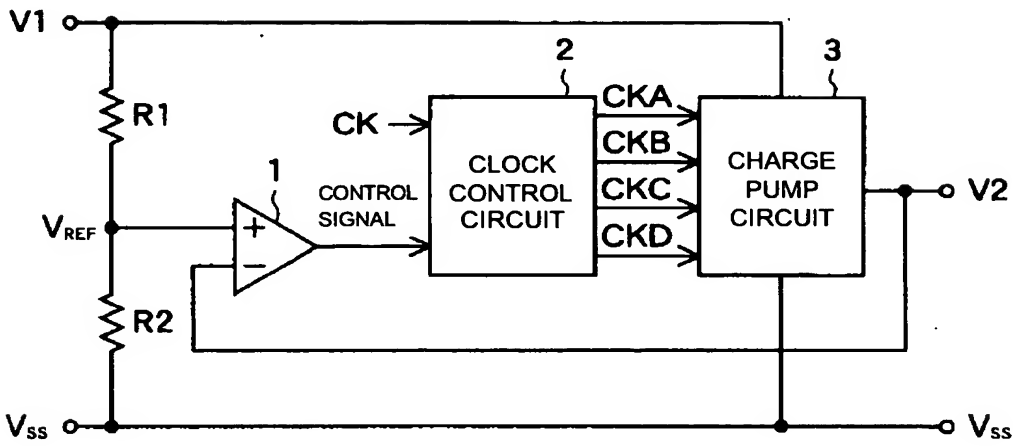

V1
R1
VREF
R2
Vss
1
CONTROL SIGNAL
CK
2
CLOCK CONTROL CIRCUIT
CKA
CKB
CKC
CKD
3
CHARGE PUMP CIRCUIT
V2
Vss

FIG. 2

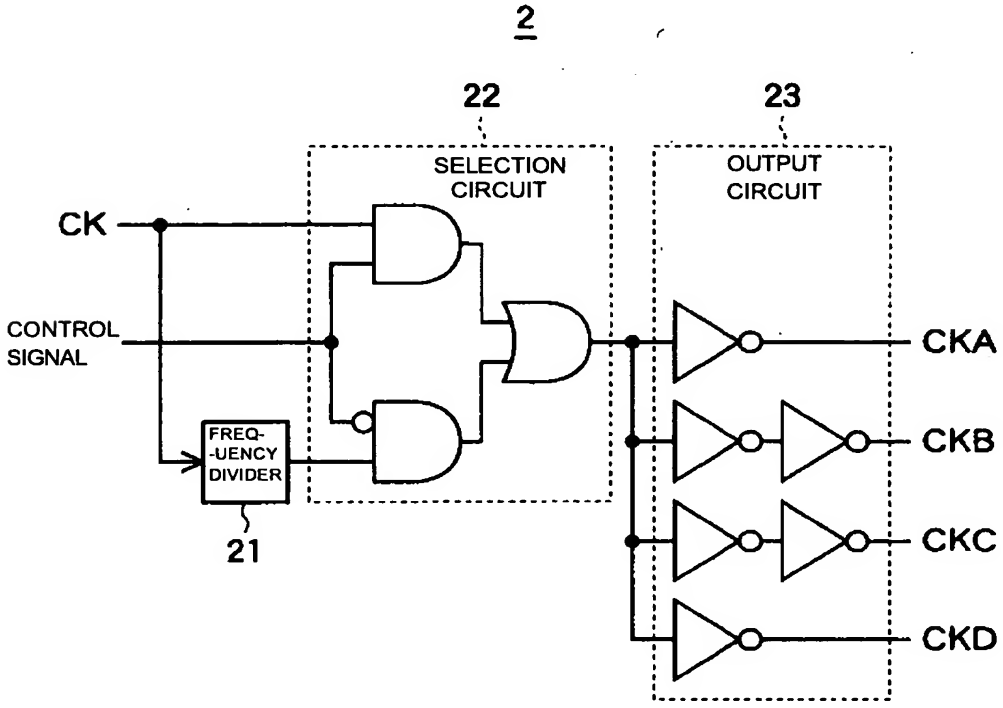

2
22
SELECTION CIRCUIT
23
OUTPUT CIRCUIT
CK
CONTROL SIGNAL
FREQ--UENCY DIVIDER
21
CKA
CKB
CKC
CKD

FIG.3

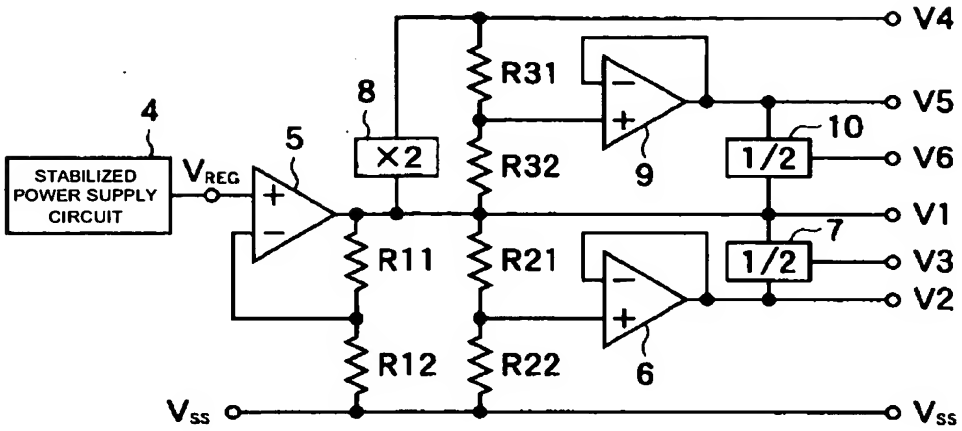

V4
R31
8
4
5
V5
10
STABILIZED POWER SUPPLY CIRCUIT
V_{REG}
×2
R32
9
1/2
V6
V1
7
R11
R21
1/2
V3
V2
R12
R22
6
V_{SS}
V_{SS}

FIG.4

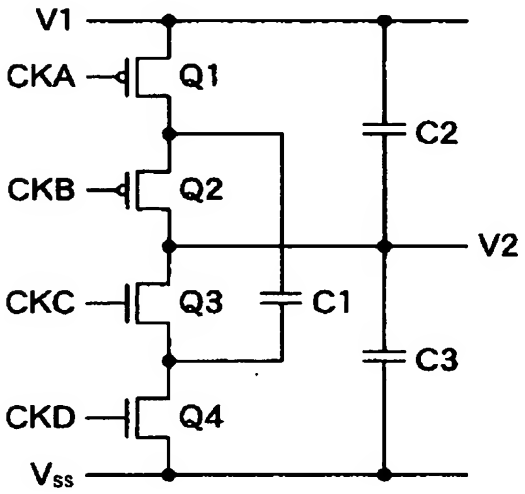

V1
CKA
Q1
C2
CKB
Q2
V2
CKC
Q3
C1
C3
CKD
Q4
V_{SS}

FIG.5

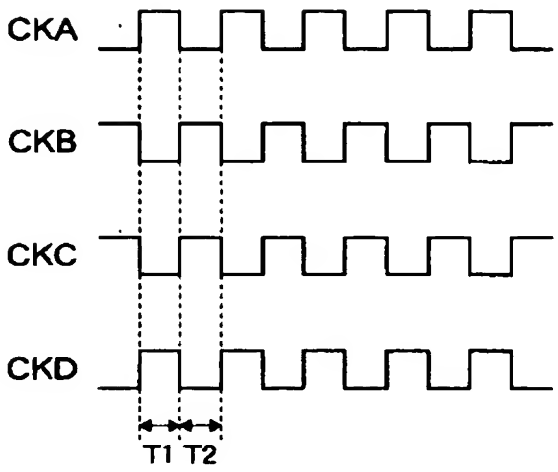


FIG.6 (a)

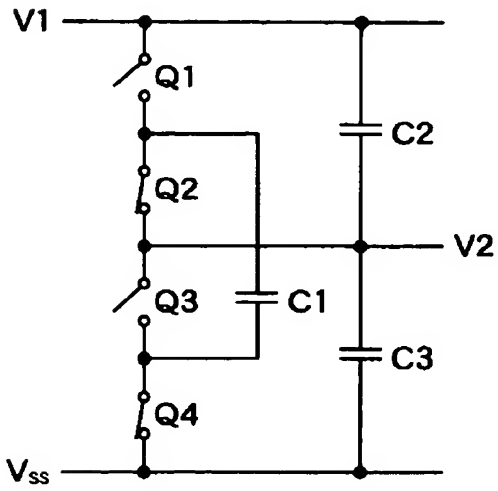


FIG.6 (b)

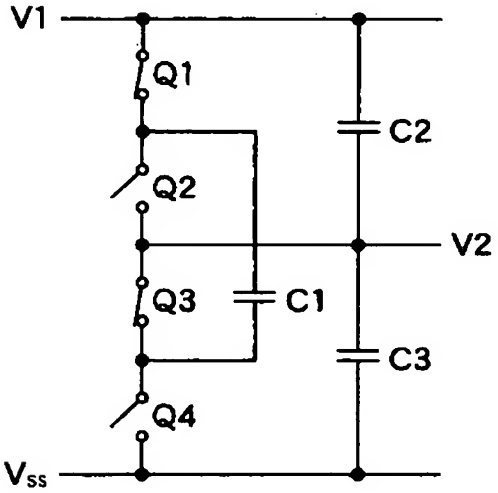
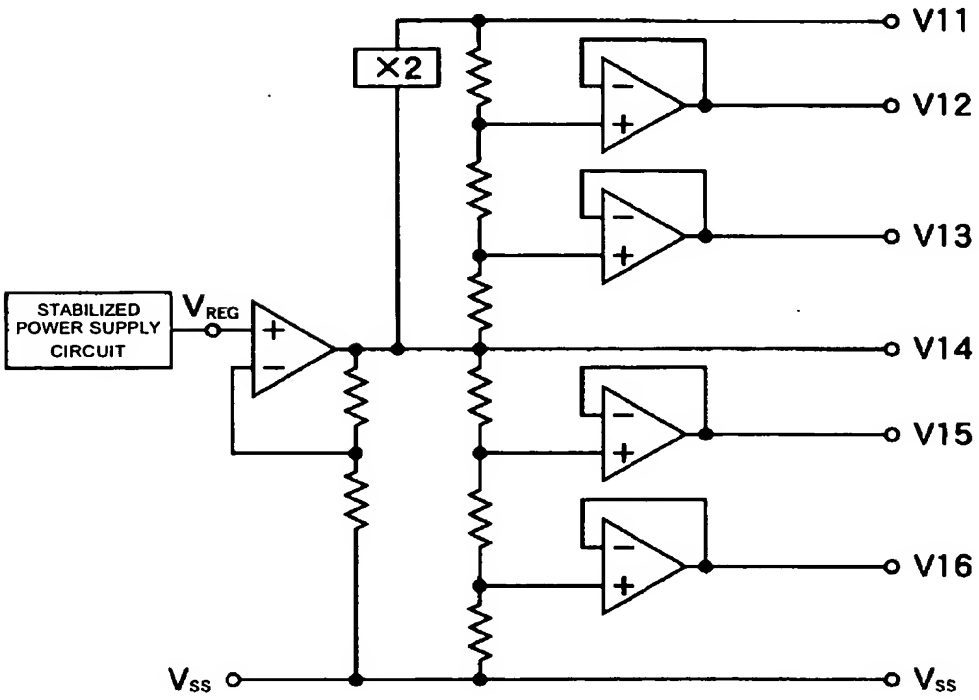


FIG.7


V11
V12
V13
V14
V15
V16
×2
STABILIZED POWER SUPPLY CIRCUIT
V_{REG}
V_{SS}
V_{SS}